AMENDMENTS TO THE CLAIMS

Please amend claims 1, 9, 17 and 22-28 as follows.

Please cancel claims 10-16 without prejudice.

Please add claims 31-35 as follows.

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1. (Currently amended) A circuit, comprising:

a first control register to be loadable after the circuit is reset;

a first plurality of control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again; and

a first switch unit coupled to the first control register and the first plurality of control registers, wherein the first switch unit to output data stored by one control register of the first plurality of control registers ~~as a function of~~ based on the data loaded in the first control register.

2. (Original) The circuit of claim 1, wherein the first switch unit comprises a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register.

3. (Original) The circuit of claim 1, wherein the first control register is loadable through software control after the circuit is reset.

4. (Original) The circuit of claim 3, wherein the software control to cause the first register to be loaded with different data in response to a change in the circuit's operational mode.

5. (Original) The circuit of claim 1, wherein the circuit is a memory controller.

6. (Original) The circuit of claim 1, wherein the first plurality of control registers to be loaded by a basic input output system (BIOS) during an initialization process after the circuit is reset.

7. (Original) The circuit of claim 6, wherein the first plurality of control registers to be locked by the BIOS during the initialization process after the circuit is reset.

8. (Original) The circuit of claim 7, wherein the first plurality of control registers each include a lock bit to be set by the BIOS to lock the first plurality of control registers during the initialization process after the circuit is reset.

9. (Currently amended) The circuit of claim 1, further comprising:

a second control register to be loadable after the circuit is reset;

a second plurality of control registers to be loadable during the initialization process and to be unloadable until the circuit is reset again; and

a second switch unit coupled to the second control register and the second plurality of control registers, wherein the second switch unit to output data stored by one control register of the second plurality of control registers ~~as a function of~~ based on the data loaded in the second control register.

Claims 10-16 (Cancelled)

17. (Currently amended) A method, comprising:

storing first data and second data in a circuit, the second data including a plurality of portions, wherein, after the circuit is reset and initialized, the first data is changeable and the second data is not changeable; and

selecting one portion of the plurality of portions in response to the first data, wherein the selected portion to be provided to ~~another unit of the circuit~~ one of a thermal control unit or a power conservation unit of the circuit.

18. (Original) The method of claim 17, further comprising changing the first data in response to software control.

19. (Original) The method of claim 18, wherein the software control causes the first data to be changed in response to a change in the circuit's operational mode.

20. (Previously presented) The method of claim 17, wherein storing second data comprises:

storing the second data by a basic input output system (BIOS) while the circuit is initialized.

21. (Previously presented) The method of claim 21, wherein the BIOS locks one or more control registers storing second data to prevent changes to the second data after the circuit is initialized.

22. (Currently amended) A method, comprising:

loading a plurality of control registers of a circuit, the plurality of control registers including a plurality of protected registers and unprotected registers, wherein the plurality of

protected control registers are loaded with sensitive data for use by a unit of the circuit, the unit to operate in accordance with the sensitive data to prevent damage to the circuit;

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locking the plurality of protected control registers;

selecting a locked protected control register of the plurality of protected control registers based on an operational mode of the circuit; and

outputting the sensitive data stored by the selected locked protected control register to the unit.

23. (Currently amended) The method of claim 22, ~~the locked control register is selected as a function of~~ wherein the operational mode is described by data stored in an unprotected control register of the plurality of unprotected control registers.

24. (Currently amended) The method of claim 22, further comprising:

deselecting the locked control register; and

selecting another locked protected control register of the plurality of protected control registers based on a change in the operational mode of the circuit.

25. (Currently amended) ~~An~~ A circuit, comprising:

a plurality of control registers;

means for loading the plurality of control registers, the plurality of control registers including a plurality of protected registers and unprotected registers, wherein the plurality of protected control registers are loaded with sensitive data for use by a unit of the circuit, the unit to operate in accordance with the sensitive data to prevent damage to the circuit;

means for locking the plurality of protected control registers;

means for selecting a locked protected control register of the plurality of protected control registers based on an operational mode of the circuit; and

means for outputting the sensitive data stored by the selected locked protected control register to the unit.

26. (Currently amended) The circuit of claim 25~~, wherein the means for selecting selects the locked control register as a function of~~ wherein the operational mode is described by data stored in an unprotected control register of the plurality of unprotected control registers.

27. (Currently amended) The circuit of claim 25, further comprising:

means for deselecting the locked control register; and

means for selecting another locked protected control register of the plurality of protected control registers based on a change in the operational mode of the circuit.

28. (Currently amended) A system, comprising:

a processor;

a memory; and

a memory controller coupled to the processor and the memory, the memory controller comprising:

a first control register to be loadable after the memory controller is reset;

a first plurality of control registers to be loadable during an initialization process after the memory controller is reset and to be unloadable after initialization until the circuit is reset again; and

a first switch unit coupled to the first control register and the first plurality of control registers, wherein the first switch unit to output data stored by one control register of the first plurality of control registers ~~as a function of~~ based on the data loaded in the first control register.

29. (Original) The system of claim 28, wherein the first switch unit comprises a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register.

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30. (Original) The system of claim 28, wherein the first control register is loadable in response to software control after the circuit is initialized.

31. (New) The circuit of claim 1, further comprising:

a unit coupled to the first switch to operate in accordance with the data received from the one control register of the first plurality of control registers.

32. (New) The circuit of claim 31 wherein the unit includes one of a thermal control unit or a power conservation unit.

33. (New) A circuit, comprising:

a first multiplexer including a first plurality of input ports, a first output port, and a first control port;

a first non-protected control register coupled to the first control port, the first non-protected control register to be loadable after the circuit is reset;

a first plurality of protected control registers coupled to the first plurality of input ports, the first plurality of protected control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again, wherein the first multiplexer to output data stored in one protected control register of the first plurality of protected control registers in response to the data stored in the first non-protected control register; and

a thermal control unit coupled to the first output port of the first multiplexer, the thermal control unit to operate in accordance with the data outputted by the first multiplexer.

34. (New) The circuit of claim 33, further comprising:

a second multiplexer including a second plurality of input ports, a second output port, and a second control port;

a second non-protected control register coupled to the second control port, the second non-protected control register to be loadable after the circuit is reset; and

a second plurality of protected control registers coupled to the second plurality of input ports, the second plurality of protected control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again, wherein the second multiplexer to output data stored in one protected control register of the second plurality of protected control registers in response to data stored in the second non-protected control register,

wherein the thermal control unit is coupled to the second output port of the second multiplexer, the thermal control unit to operate in accordance with the data outputted by the second multiplexer.

35. (New) The circuit of claim 31, further comprising:

a third multiplexer comprising a third plurality of input ports, a third output port, and a third control port;

a third non-protected control register coupled to the third control port, the third non-protected register to be loadable after the circuit is reset;

a third plurality of protected control registers coupled to the third plurality of input ports, the third plurality of protected control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again, wherein

the third multiplexer to output data stored in one protected control register of the third plurality of protected control registers in response to data loaded in the third non-protected control register; and

a power conservation unit coupled to the third output port of the third multiplexer, the power conservation unit to operate in accordance with the data outputted by the third multiplexer.